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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent No.:	7100058
Issued:	August 29, 2006
First Named Inventor:	Jock F. Tomlinson
Title	PROGRAMMABLE POWER MANAGEMENT SYSTEM AND METHOD

**REQUEST FOR ISSUANCE OF CERTIFICATE OF CORRECTION  
PURSUANT TO 37 CFR 1.323**

Certificate of Corrections Branch  
Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

Review of the above-identified patent has revealed two errors in the patent attributable to applicants. These errors are of a clerical and typographical nature, and their proposed corrections do not constitute new matter or require reexamination. Applicants therefore request that a Certificate Of Correction be issued to correct these errors.

The locations of the errors in the patent are set forth below:

<b>Errors in Patent</b>	<b>Proposed Corrections</b>
Claim 17, line 4 ("operable to a control")	-- operable to control --
Claim 20, line 2 ("operable to a control")	-- operable to control --

**Certificate**  
APR 04 2007  
**of Correction**


APR 04 2007

Documentation supporting this request and a form PTO/SB/44 showing the corrections are enclosed.

The Commissioner is hereby authorized to charge any fees associated with this communication to Deposit Account No. 501958.

Respectfully submitted,

Date: 3/27/07

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The invention claimed is:

1. A power management integrated circuit comprising:  
a plurality of input terminals adapted to receive analog  
input voltage signals;  
a plurality of analog input monitor circuits coupled to the  
input terminals, each analog input monitor circuit oper-  
able to compare an input analog voltage received at an  
input terminal against at least one voltage reference;  
control logic coupled to the plurality of analog input  
monitor circuits and operable to generate at least one  
control signal in response to output signals from the  
analog input monitor circuits; and  
at least one FET driver circuit coupled between the  
control logic and an output terminal and capable of  
controlling a power switch, the FET driver circuit  
operable in response to a control signal from the control  
logic,  
wherein the control logic is operable, in response to an  
output signal from an analog input monitor circuit, to  
generate a ramp control signal that gradually turns on  
the FET driver circuit.
2. The integrated circuit of claim 1, wherein at least one  
analog input monitor circuit is operable to compare an input  
analog voltage against high and low voltage references.
3. The integrated circuit of claim 1, wherein at least one  
analog input monitor circuit is operable to compare a first  
input analog voltage received at a first input terminal to a  
second input analog voltage received at a second input  
terminal.
4. The integrated circuit of claim 1, wherein at least one  
analog input monitor circuit is operable to monitor the  
voltage across an external resistor by comparing the volt-  
ages, and the control logic is operable to generate an  
indicator signal in response to the output signal from the  
analog input monitor circuit.
5. The integrated circuit of claim 1 including a program-  
mable voltage reference generator.
6. The integrated circuit of claim 1 including a plurality of  
FET driver circuits, wherein the control logic is program-  
mable to generate a plurality of respective ramp control  
signals to turn on the FET driver circuits in a programmed  
sequence.
7. The integrated circuit of claim 1, wherein the control  
logic is programmable.
8. The integrated circuit of claim 7, wherein the control  
logic includes a plurality of macrocells.
9. The integrated circuit of claim 1, wherein the FET  
driver circuit is programmable.
10. The integrated circuit of claim 1 including a charge  
pump circuit coupled to the FET driver circuit.
11. The integrated circuit of claim 1, wherein the FET  
driver circuit comprises an FET driver circuit capable of  
driving a power MOSFET switch coupled to the output  
terminal.
12. The integrated circuit of claim 1 including a serial  
interface coupled to the control logic and operable to support  
the I<sup>2</sup>C protocol.

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13. The integrated circuit of claim 7 including nonvolatile  
programmable memory operable to store information for  
configuring the control logic.
14. The integrated circuit of claim 1 including a watchdog  
timer coupled to the control logic and operable to monitor a  
time-based event.
15. The integrated circuit of claim 1, wherein the control  
logic is operable to provide a plurality of selectable ramp  
control signals that vary in the rate at which they turn on the  
FET driver circuit.
16. The integrated circuit of claim 1, wherein the ramp  
control signal is generally monotonic and linear.
17. A power management integrated circuit comprising:  
a plurality of analog input monitor circuits operable to  
sense a plurality of power supply output signals;  
a plurality of FET driver circuits operable to a control,  
respectively, a plurality of power switches of the type  
coupled to output terminals of a power supply; and  
programmable control logic coupled to the input monitor  
circuits and to the FET driver circuits, the control logic  
configurable to turn on the plurality of FET driver  
circuits in a programmed sequence and in response to  
output signals of the analog input monitor circuits  
wherein the control logic is programmable to provide  
ramp control signals that gradually turn on the FET  
driver circuits.
18. The integrated circuit of claim 17, wherein the control  
logic is operable to provide a plurality of selectable ramp  
control signals that vary in the rate at which they turn on  
each FET driver circuit.
19. The integrated circuit of claim 17 including nonvola-  
tile programmable memory operable to store information for  
configuring the control logic.
20. A power management integrated circuit comprising:  
a plurality of FET driver circuits operable to a control,  
respectively, a plurality of power switches of the type  
coupled to output terminals of a power supply; and  
programmable control logic coupled to the FET driver  
circuits, the control logic configurable to turn on the  
FET driver circuits in a programmed sequence,  
wherein the control logic is operable, in response to  
sensing of power supply signals, to generate ramp  
control signals that gradually turn on the FET driver  
circuits in the programmed sequence.
21. The integrated circuit of claim 20, wherein the control  
logic is operable to provide a plurality of selectable ramp  
control signals that vary in the rate at which they turn on  
each FET driver circuit.
22. The integrated circuit of claim 20, wherein the FET  
driver circuits are programmable.
23. The integrated circuit of claim 20 including nonvola-  
tile programmable memory operable to store information for  
configuring the control logic.

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CERTIFICATE OF CORRECTION**Page 1 of 1

PATENT NO. : 7,100,058

APPLICATION NO.: 10/726,972

ISSUE DATE : August 29, 2006

INVENTOR(S) : Tomlinson et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 17, line 4: replace "operable to a control" with -- operable to control --.

Claim 20, line 2: replace "operable to a control" with -- operable to control --.

**MAILING ADDRESS OF SENDER (Please do not use customer number below):**

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This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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